REMARKS

This is in full and timely response to the Office Communication dated August 20, 2009.

Claims 7-22 are currently pending in this application, with claim 7 being independent.

No new matter has been added.

Reexamination in light of the following remarks is respectfully requested.

Entry of amendment

This amendment *prima facie* places the case in condition for allowance. Alternatively, it places this case in better condition for appeal.

Accordingly, entry of this amendment is respectfully requested.

Prematureness

Applicant, seeking review of the *prematureness* of the final rejection within the Final Office Action, respectfully requests reconsideration of the finality of the Final Office Action for the reasons set forth hereinbelow. See M.P.E.P. §706.07(c).

At least for the following reasons, if the allowance of the claims is not forthcoming at the very least and a new ground of rejection made, then a ***new non-final Office Action*** is respectfully requested.

Claim rejections

Paragraph 3 of the Final Office Action indicates a rejection of claims 7-21 as allegedly being unpatentable over the "Background Art" of the specification for the present application (AAPA) in view of Japanese Application Publication No. 2002-009594 (Iemoto).

Paragraph 19 of the Final Office Action indicates a rejection of claim 22 as allegedly being unpatentable over AAPA and Iemoto in view of U.S. Patent No. 6,897,909 (Ochiai).

This rejection is traversed at least for the following reasons.

Claims 7-22 - Claims 8-22 are dependent upon claim 7. Claim 7 is drawn to a display device comprising:

> a level shifter configured to change an amplitude of gradation data from a first voltage range to a second voltage range, amplified gradation data being said gradation data at said second voltage range,
>
> wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.

AAPA – The Office Action contends that AAPA discloses the presence of a level shifter (fig. 1 (1)) (Office Action at page 2).

However, the Office Action ***readily admits*** that AAPA ***fails*** to teach wherein output data during a quiescent period is dummy data (Office Action at page 3).

- ***Thus, AAPA fails to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.***

Iemoto – The Office Action cites Iemoto for the features that are admittedly absent from within Iemoto.

In response, the machine translation of Iemoto arguably discloses the following at paragraph [0010]:

> [0010]Although *the **vernier 10** is a circuit which acquires a time delay with the variable resolution below a reference signal*, since it has a time delay more than the cycle of a reference signal at least including the fixed delay of a vernier at the time of maximum delay setting out, compared with other logic gates, the delay time variations to a temperature change will become large.

The machine translation of Iemoto arguably discloses the following at paragraphs [0024]-[0026]:

> [0024]The delay circuit 32 is larger than the time delay of the flip-flop 20, and delays the inputted reference signal RCLK within the time of the cycle T and the difference of pulse width of the reference signal RCLK, and *outputs **delay clock signal DCLK** to OR gate 50 **as a dummy pulse signal***.
>
> [0025]OR gate 50 carries out OR operation of the ***delay clock signal DCLK*** inputted as signal TM2 inputted from the flip-flop 20 from the delay circuit 32, and outputs it to the vernier 10 as ***mix-signals TD3***.
>
> [0026]*The vernier 10 delays **mix-signals TD3*** inputted from OR gate 50 according to a preset value by the time resolution below the cycle T of the reference signal RCLK, and *outputs it* to the delay circuit 42 and the flip-flop 41 as *delay pulse signal TD4*.

However, Iemoto ***fails*** to disclose, teach, or suggest ***mix-signals TD3*** as including amplified gradation data.

- ***Thus, Iemoto fails to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.***

Combination of AAPA and Iemoto as a whole – The Office Action contends that it would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the dummy data during a quiescent period as taught by Iemoto in order to reduce fluctuations in the operating frequency of the circuit as stated in the abstract of Iemoto (Office Action at page 3).

1. In response, the Office Action ***fails*** to show the time periods for the alleged quiescent period of AAPA and the alleged quiescent period of Iemoto as being one in the same.

2. The Office Action apparently attempts an association of the output data D2 of AAPA with the claimed amplified gradation data (Office Action at page 2).

Likewise, the Office Action attempts an association of the delay clock signal DCLK of Iemoto with the claimed dummy data (Office Action at page 3).

Claim 7 includes a level shifter configured to change an amplitude of gradation data from a first voltage range to a second voltage range, amplified gradation data being said gradation data at said second voltage range.

Iemoto ***fails*** to disclose the presence of a level shifter.

As a consequence, the Office Action ***fails*** to show how and why the skilled artisan would have considered any of the mix-signals TD3 of Iemoto as including ***amplified*** gradation data.

3. The Office Action ***fails*** to show the alleged output data of AAPA and the alleged output data of Iemoto as being one in the same.

4. The Office Action ***fails*** to show where and how the level shifter 1 of AAPA would have been integrated into the circuitry of Iemoto.

5. The Office Action ***fails*** to show where and how the output data would have been gradation data from AAPA in one instance and any of the mix-signals TD3 from Iemoto in the next instance, especially when there is no disclosure of time T2 of AAPA within Iemoto.

Ochiai – Ochiai arguably discloses that the term "polysilicon" also encompasses macrocrystalline silicon and ***continuous grain silicon (CGS)*** as well as single-crystal silicon (Ochiai at column 23, lines 48-50).

- ***However, Ochiai fails to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.***

Allowance of the claims is respectfully requested.

Official Notice

There is no concession as to the veracity of Official Notice, if taken in any Office Action.

An affidavit or document should be provided in support of any Official Notice taken. 37 CFR 1.104(d)(2), MPEP § 2144.03. See also, *Ex parte Natale*, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989)(failure to provide any objective evidence to support the challenged use of Official Notice constitutes clear and reversible error).

Extensions of time

Please treat any concurrent or future reply, requiring a petition for an extension of time under 37 C.F.R. §1.136, as incorporating a petition for extension of time for the appropriate length of time.

Fees

The Commissioner is hereby authorized to charge any deficiency in fees filed, asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm).

The Commissioner is hereby authorized to charge all required fees, fees under 37 C.F.R. §1.17, or all required extension of time fees.

If any fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Conclusion

This response is believed to be a complete response to the Office Action.

Applicants reserve the right to set forth further arguments supporting the patentability of their claims, including the separate patentability of the dependent claims not explicitly addressed herein, in future papers.

For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance.

Accordingly, favorable reexamination and reconsideration of the application in light of the remarks is courteously solicited.

If the Examiner has any comments or suggestions that could place this application in even better form, the Examiner is requested to telephone Brian K. Dutton, Reg. No. 47,255, at 202-955-8753.

Dated: October 13, 2009

Respectfully submitted,

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